REMARKS

This Amendment is in response to the Office Action mailed April 6, 2004. In the Office Action, the Examiner rejected claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Summary of Telephonic Interview

Applicant thanks the Examiner for the courtesy of a telephonic interview on June 16, 2004. Claim 1 was discussed in view of the disclosure of Ross et al. (US 5,915,117). Applicant inquired as to whether the gravamen of the pending rejection was that the Examiner construed applicant's pending claim element of a "memory load request issued by the executing program to retrieve the memory value from the memory" to read on loading of an instruction as disclosed by Ross. The Examiner agreed that the claim was so construed in rejecting the claim over the disclosure of Ross. Applicant asked if an amendment to the claim that distinguished the loading of data to be used by an instruction from the loading of an instruction might overcome the rejection based on Ross. The Examiner agreed that such an amendment did have the potential to overcome the presently outstanding rejection.

Rejection Under 35 U.S.C. § 102

The Examiner rejects claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102(b) as being anticipated by Ross et al. (US 5,915,117).

Following the telephonic interview with the Examiner, applicant has further studied the disclosure of Ross. Applicant now submits that the claimed invention is more properly distinguished from Ross by the nature of the event handled rather than by the nature of what is loaded to cause the event as further discussed below.

As per claim 1, the Examiner asserts that Ross discloses a method of handling memory errors, in the form of memory exceptions. Col. 1, lines 13-16.

Applicant has amended claim 1to make clear that the invention is directed to handling memory errors caused by corruption of the content of a particular memory location as described in the "Background of the Invention" of the specification as filed.

As used in Ross, the term "exception" is generally understood to mean an error that is reported to the program that issued the instruction for handling. See Pentium Pro Family Developer's Manual, Volume 2, copyright date 1997, pages 4-10 through 4-15 (Developer's Manual) submitted herewith. The exception mechanism allows programs to consolidate error handling because the exception triggers a change of the program flow. Exception handling is an alternative to returning a completion code that requires the program to explicitly check the code on every return.

Ross notes that the speculative execution of instructions that may throw an exception is problematic. Col. 1, line 58, through Col. 3, line 25. It is significant that the nature of exceptions is that they reflect the occurrence of an event that the calling program can deal with.

Often the calling program is the only place that graceful recovery from the exception is possible. Table 4-1 on page 4-11 of Developer's Manual is a representative list of the types of events that throw exceptions. It should be observed that a memory error caused by corruption of the content of the memory location being loaded does not throw an exception. Corruption of memory values is neither caused by the program nor is it correctable by the program. In contrast errors such as a General Protection Fault, which may mean that the program has generated an invalid memory reference, or a Page Fault, which may mean that the Page Tables need to be loaded, can or must be handled by the calling program if the program is not to be aborted. Corrupt memory values must be corrected by the memory hardware if they are to be corrected at all. Uncorrectable memory errors lead to a program abort.

Applicant respectfully submits that claim 1 as amended to include the element of handling memory errors caused by corruption of the content of a particular memory location clearly distinguishes the present invention from the disclosure of Ross which is directed to deferring exception processing by the executing programs.

As per claims 2 and 3, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

As per claims 6-8, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 11-13, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 16-18, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102(b) as being anticipated by Ross.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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